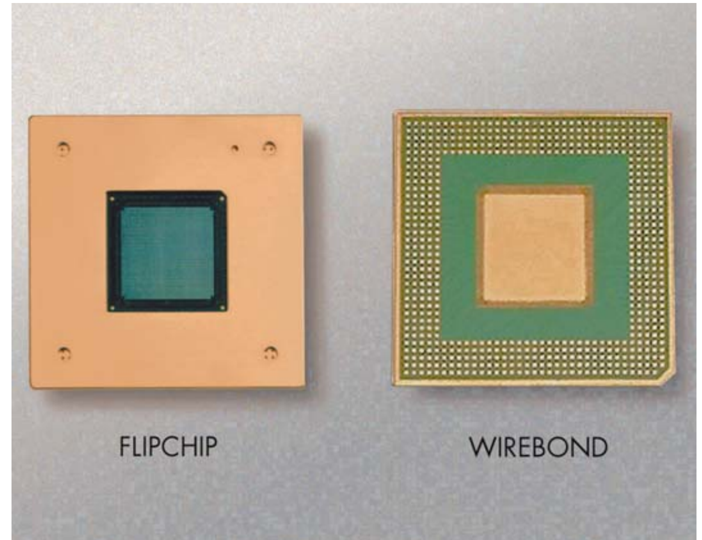
GORE™ G410 PREPREG DATA SHEET

GORE G410 Prepreg allows production of reliable, high performance, single-chip substrate packages using modified printed circuit board construction techniques. GORE G410 delivers the high performance organic substrate at a reasonable cost.



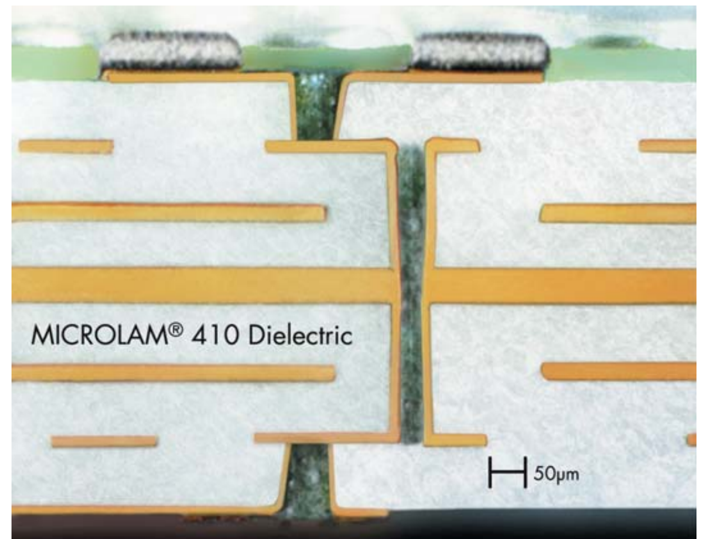
Photograph courtesy of 3M Company

Advantages

- Excellent dimensional stability for fine line processing
- Stable Dk and Df over a wide frequency range
- CTE matched to copper in X, Y, and Z-axis, allowing high aspect ratio vias
- Superior thickness control for superior power distribution impedance
- Proven moisture reliability
- High Tg (225°C)
- Processes with standard PWB techniques

Typical Applications

- Thin-core and coreless chip package substrates
- Telecom and computing ASIC
- Wirebond and flipchip SCM and MCM



W. L. Gore & Associates

North America:
1 (800) 445-4673
International:
1 (302) 292-5100

Europe:
+49/91 44/6010
+44/1392-561511
www.gore.com/electronics

GORE
Creative Technologies Worldwide

Typical Material Properties

Property		Method	Value*
Dielectric constant	500 MHz	Split post resonant cavity	3.4
	10 GHz	Kent cavity	3.4
	40 GHz	DI Model 600T Open Resonator	3.3
Loss tangent	500 MHz	Split post resonant cavity	0.008
	10 GHz	Kent cavity	0.008
	40 GHz	DI Model 600T Open Resonator	0.008
Glass transition temperature (Tg)		TMA	220°C
Coefficient of thermal expansion (CTE)		TMA (–55 to +125°C)	19 ppm/°C (X, Y, Z)
Thermal conductivity		(–67 to +257°F) ASTM E1530 at 20°C (68°F)	0.46 W/mK
Flammability		UL	94 V-0**
Tensile modulus		at 25°C (77°F)	12.2 GPa
Moisture absorption		24-hr. immersion, 20°C	0.17 % w/w
Peel strength		IPC TM650 Method 2.4.9 17 µm copper (1/2 oz)	0.6 Kg/cm
Pressed thickness		IPC TM650 Method 2.4.38	63 µm

* Typical properties are not specification limits, but nominal performance values

** Tested to UL flammability requirements by an independent lab

Substrate Reliability Information

Item	Test Method	Condition	Result
Preconditioning	JEDEC JESD22-A113A Level 3	30°C; 60% RH; followed by 3 reflows at 225°C	Pass
Thermal shock	JESD22-A106A Condition C	15 cycles; –55°C to +125°C; liquid-to-liquid	Pass
Thermal cycling	JESD22-A104A Condition B	3,000 cycles; –55°C to +125°C; air-to-air	Pass
Pressure cooker test	JEDEC JESD22-A102B	168 hrs; 15 psig; 121°C	Pass
High temperature storage	JESD22-A103A	150°C; 1,000 hrs	Pass
Temperature humidity bias (THB)	JEDEC JESD22-A101A	85°C; 85% RH; 1,000 hrs; 5V bias	Pass
Solderability	MIL-STD-883 Method 2003	8 hrs steam aging; in solder followed by immersion	Pass
HAST	JESD22-A110A	130°C; 85% RH; 5V; 96 hrs	Pass

MICROLAM is a trademark of W. L. Gore & Associates, Inc.

The information given herein is based on data believed to be reliable. However, W. L. Gore & Associates, Inc. makes no warranties, expressed or implied, as to its accuracy and assumes no liability arising out of its use by others. This publication is not to be taken as a license to operate or as a recommendation to infringe patents.

W. L. Gore & Associates

North America:
1 (800) 445-4673
International:
1 (302) 292-5100

Europe:
+49/91 44/6010
+44/1392-561511
www.gore.com/electronics

© 2004 W. L. Gore & Associates

Gore and Design are trademarks of W. L. Gore & Associates.